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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MURALIDAR, RICHARD V	

ART UNIT	PAPER NUMBER
2838	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,245	DATE ET AL.	
	Examiner	Art Unit	
	RICHARD V. MURALIDAR	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-16,21 and 22* is/are rejected.

7)☒ Claim(s) *17-20 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/10/2007, 9/14/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to the response to election/restriction filed 02/15/2008. Applicant's election of species II (readable on claims 12-23; Figures 4, 5, and 6) without traverse is acknowledged.

Drawings

Figures 20 and 23 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Figures 21A-D and 22A-D also appear to be prior art. If so please label accordingly. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description**: Figure 5 lists items 45, 63, 65, and 67 with no corresponding names given in the specification.** Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet

should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12-16, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over [U.S. 6456270] in view of [U.S. 6882186].

With respect to claim 12, Itakura discloses a current driving device [col. 2 lines 35-63] comprising: a first-conductive-type first MISFET [Fig. 18, MB1] in which a reference current flows in a driving state; a first-conductive-type first current distribution MISFET [Fig. 18, MB2] which constitutes a current mirror circuit together with the first MISFET and makes the reference current flow; a second-conductive-type first current input MISFET [Fig. 18, MF1] having a drain connected to the first current distribution MISFET; and a plurality of current supply sections [Fig. 18, 124-1 to 124-n] each including second-conductive-type current source MISFETs [Fig. 18, M2] constituting a

current mirror circuit together with the first current input MISFET, switches [Fig. 18, pixel driving switches are connected to the output terminals of M1, M2, etc.] which are connected to the current source MISFETs and turn ON or OFF a current flowing in the current source MISFETs in accordance with display data [col. 3 lines 10-67], and an output terminal [Fig. 18, the output terminals of M1, M2, etc.] which is connected to the switches and outputs a current in accordance with the display data to a display panel, the current driving device being provided on a semiconductor chip [col. 5 lines 48-57].

Itakura does not disclose that a plurality of units of the first current distribution MISFET and the first current input MISFET are provided for the semiconductor chip, and wherein a bias line connected to a gate electrode of the first MISFET and gate electrodes of the first current distribution MISFETs and shared by the gate electrodes is further provided.

Nishitoba discloses a plurality of units [Tr2-Trn] of the first current distribution MISFET and the first current input MISFET are provided for the semiconductor chip, and wherein a bias line connected to a gate electrode of the first MISFET and gate electrodes of the first current distribution MISFETs and shared by the gate electrodes is further provided [Fig. 7, bias line connecting Tr0 to Trn+1].

Itakura and Nishitoba are analogous current display drivers. It would have been obvious to one of ordinary skill in the art at the time of the invention to equip each of the plurality of current supply sections [Itakura, Fig. 18, 124-1 to 124-n] with its own dedicated power supply [Nishitoba, plurality of units Tr2-Trn], as taught by Nishitoba, for the benefit of providing each pixel driving circuit with an independent and sufficient

source of current to uniformly and brightly light each display pixel. One of ordinary skill would use MISFETS/MOSFETS [A MOSFET is a type of MISFET] as taught by Itakura to implement the plurality of units Tr2-Trn, as taught by Nishitoba, for the benefit of faster response time and ease of integration into IC chip technology.

With respect to claim 13, Itakura discloses all of respective gate electrodes of the current source MISFETs in the plurality of current supply sections and a gate electrode of the first current input MISFET are connected to one another [Fig. 18, the gate electrodes of M1-Mn are connected to a single bias line coming from MA-12].

With respect to claim 14, Nishitoba discloses each of the plurality of current supply sections [Fig. 8, 20A] includes a second- conductive-type first cascode MISFET [Fig. 8, 22 implemented as MISFET/MOSFET] which is provided between each of the switches and the output terminal and is turned ON when a voltage equal to or lower than a power supply voltage of the display panel is applied to a gate electrode in a driving state.

With respect to claim 15, Itakura discloses each of the switches is a second cascode MISFET which forms a cascode connection together with the current source MISFETs and is controlled to be turned ON or OFF depending on whether or not a predetermined voltage is applied to a gate electrode in a driving state [Fig. 1, any of the matrix switches shown].

With respect to claim 16, the combination of Nishitoba and Itakura produces these limitations. See the remarks above.

With respect to claim 21, Itakura discloses wherein on the semiconductor chip, a plurality of MISFET regions each collectively including the current source MISFETs are arranged in a row [Fig. 1], and wherein each of the plurality of current supply sections includes MISFETs arranged in at least two of the MISFET regions [Fig. 2, 2 MISFETS per current supply section].

With respect to claim 22, Nishitoba discloses a resistance element provided on the bias line and between respective gate electrodes of adjacent ones of the current distribution MISFETs [Fig. 7, the resistance element is the bias line itself, which will provide resistance].

Allowable Subject Matter

Claims 17-20 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

Claim 17 is allowed because the prior art does not teach or suggest: "between each of the first current distribution MISFETs and each of the first current input MISFETs, connection changing means for changing a connection so that each of the first current distribution MISFETs is connected to a different one of the current input MISFETs in every arbitrary period." Claims 18-20 depend from 17.

Claim 23 is allowed because the prior art does not teach or suggest" "a plurality of first-conductive-type third current distribution MISFETs for transmitting the reference

current in a driving state; a plurality of second-conductive-type second current input MISFETs each having a gate electrode connected to an associated one of respective gate electrodes of the plurality of third current distribution MISFETs and a drain connected to an associated one of respective drains of the plurality of third current distribution MISFETs; and a second-conductive-type third cascode MISFET which constitutes a current mirror circuit together with the second current input MISFETs and is provided between the current source MISFETs and one of the switches."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD V. MURALIDAR whose telephone number is (571)272-8933. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Akm E. Ullah can be reached on 571-272-2361. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Richard V. Muralidar/
Examiner, GAU 2838
5/10/2008

/Bao Q. Vu/
Primary Examiner, Art Unit 2838
May 12, 2008